

## Patent Claims:

1. A circuit arrangement for holding a relay, in  
5 which
  - the current for the pull-in of the relay is supplied by a first DC source (J1), and in which this current flows via a first controllable switch (S1) connected in series with the first DC source (J1),
  - 10 - a second DC source (J2) connected in parallel with the first source is provided, which feeds the relay winding, after the relay has pulled in, via a second controllable switch (S2) connected in series with said source,
  - 15 - with the aid of a threshold value switch (Sw) and a logic device (LE), the two controllable switches (S1, S2) are set in such a way that, after the relay has pulled in, the first controllable switch (S1) is opened and the second (S2) is closed,
  - 20 characterized
    - a) in that a controllable resistor (Rs) is connected in parallel with the first controllable switch (S1), the value of which resistor is influenced by a regulator (Rg),
    - 25 b) in that the regulator (Rg) becomes active only when the first controllable switch (S1) is open and the second controllable switch (S2) is closed,
    - c) in that, when the current (i) through the relay winding falls below a predetermined value ( $i_r$ ) the regulator (Rg) regulates said current to the
    - 30 predetermined value ( $i_r$ ) with the aid of the controllable resistor (Rs).
2. The circuit arrangement as claimed in claim 1,  
35 characterized in that the regulator (Rg) has a D action.
3. The circuit arrangement as claimed in claim 1,

characterized in that the controllable resistor (Rs) serves as a switching amplifier (T1, T2) for switching the first DC source (J1).

- 5 4. The circuit arrangement as claimed in claim 1, characterized in that the threshold value switch (SW) and the regulator (Rg) have a common input transistor stage (T5).
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The invention relates to a circuit arrangement for holding a relay having the further features specified in the preamble of claim 1.

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In switched communication technology, relays having a low-resistance and a high-resistance winding are customary for relay circuits with different pull-in and holding conditions. In this case, the low-resistance winding has 60  $\Omega$ , for example, and the high-resistance winding 1000  $\Omega$ . The relay is pulled-in via the high-resistance winding; the low-impedance winding can be connected in series in this case. After the relay has pulled in, the high-resistance winding is short-circuited by auxiliary contacts of the relay, for example, and a resistor is inserted in series with the low-resistance winding, which resistor sets the current through the low-resistance winding to the value of the holding current. The holding winding has a low resistance in order that specific locking functions can be carried out, for example the prevention of double testing of a selector. If the holding excitation is significantly smaller than the pull-in excitation in the case of a relay as well, then the holding current can nevertheless have a similarly high value to that of the pull-in current owing to this low-resistance nature. Such a high value of the holding current has the disadvantage that rather a lot of energy is drawn

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from the current source. This has a very disadvantageous effect particularly in the case of a switching system with many relay arrangements of this type. In this case, the current source is, for example,  
5 the station battery with a terminal voltage of 60 volts and a nonreactive resistor connected in series.

It is conceivable, in order to reduce the power loss, after the relay has pulled-in, to changeover to a  
10 holding circuit fed with a lower terminal voltage by a DC source. Such a measure with a reduced terminal voltage has the disadvantage, however, that the required holding current for the relay can be undershot more easily if a superposed interference voltage occurs  
15 in the electric circuit. Such an interference voltage can arise particularly when a transmission core is coupled to a specific point in the holding circuit. The C core of a switched connection system shall be mentioned as an example thereof. A ground voltage on  
20 said core effects the pull-in of a specific relay, also called test relay, in the calling switching center. Said relay initiates the setup of a switched connection and is in the pulled-in state for the duration of this connection that has been set up. Removal of the ground  
25 voltage on the associated C core effects the drop-out of the test relay and thus the clear-down of the switched connection. An interference voltage of corresponding amplitude and frequency superposed on  
said C core can therefore cause such a clear-down in  
30 the case of unfavorable dimensioning of the holding circuit.

US-A 37 86 314 describes a circuit arrangement which influences the current flow through a coil which, for  
35 its part, may be part of an electromagnetically actuated device, e.g. a relay. Only one voltage source is used in this arrangement. A voltage regulator ensures that the DC voltage dropped across the coil

remains constant until the coil current has exceeded a threshold value. A further regulating circuit then undertakes the regulation of the current through the coil and holds said current at a value which is less  
5 than the threshold value.

DE-B 12 03 314 discloses a circuit arrangement with which an inductance is intended to be switched on rapidly and to be held in the switched-on state with  
10 the lowest possible power demand. The circuit arrangement comprises two voltage sources with different source voltages, a threshold value switch and a logic unit, by which two switches are controlled. By means of the first switch, the inductance is firstly  
15 connected to the voltage source having the higher source voltage. If the current through the inductance has then exceeded a threshold value, the threshold value switch and the logic unit are used to disconnect the first voltage source from the coil and at the same  
20 time undertake the supply of current to the second voltage source. Regulation of the holding current is not provided.

Taking the prior art described as a departure point, it  
25 is an object of the invention to specify an arrangement of the type mentioned in the introduction which is as insensitive as possible to interference voltages which might cause a drop-out of the relay.

30 This object is achieved by means of the features specified in the characterizing part of claim 1.

The invention will be described and explained in more detail below using an exemplary embodiment. In the  
35 figures:

Figure 1 shows the basic circuit diagram of the circuit arrangement according to the invention,

Figure 2 shows the schematic circuit diagram of the exemplary embodiment,

Figure 3 shows the timing diagram for representing the action of the exemplary embodiment.

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In the basic circuit diagram in accordance with figure 1, the voltage source U1 and the resistor R1 form the first current source (J1) and the voltage source U2 and the resistor R2 form the second current source (J2).

10 The current source J1 can be connected via the switch S1 and the current source J2 via the switch S2. The pull-in of the relay P is effected with switch S1 closed by the closing of the switch S. This switch S is formed by the contacts of a selector, for example. If  
15 the relay P has pulled-in, then the current flowing through the relay winding, designated as relay current  $i$  hereinafter, triggers a signal at the output Sw1 of the threshold value switch Sw. This signal drives the input LE1 of the logic device LE which, for its part,  
20 disconnects the current source J1 via the output LE2 and also the switch S1 and connects the current source J2 via the output LE3 and also the switch S2. If the relay current  $i$  supplied by the current source J2 falls below a specific value, then a voltage which rises as  
25 the magnitude of this undershoot increases occurs at the output RG1 of the regulator RG. This voltage controls the controllable resistor RS from the value  $\infty$  to a corresponding finite value. As a result of this measure, the amount of current taken from the current  
30 source J1 and added to the current of the current source J2 is such that the relay current  $i$  is fixed at the specific value required for the duration of the undershoot. The connecting line from the output LE3 of the logic device LE to the input Rg2 of the regulator  
35 Rg is intended to have the effect that the latter is activated only during the holding state of relay P.

The exemplary embodiment in accordance with figure 2

relates to the signaling converter of a time division multiplex system which is arranged between two group selection stages of a switching system. Such signaling converters serve for sampling the switching identifications and for uncoded or coded transmission of the samples via the time division multiplex system. At the receiving end, said samples are converted back into the original form of the respective switching identification. A distinction is made, in accordance with the set up direction of the switched connection, into an "outgoing" converter, which is situated at the calling end of the time division multiplex system, and into an "incoming" signaling converter which is arranged at the called end of the time division multiplex system. In the present case, the circuit arrangement according to the invention is part of the "outgoing" signaling converter. This signaling converter must be able to carry out the functions "testing", "seizure" and "blocking" in conjunction with the group selector connected upstream, like a normal group selector. In the group selector connected upstream, designated here by GW, these functions are carried out with the aid of a test relay P. This test relay P operates, in principle, like the test relay described in the introduction. The interaction between the group selector GW and the downstream "outgoing" signaling converter will be discussed briefly below with the aid of figure 2. The group selector GW firstly checks whether the signaling converter is ready for seizure. Ready for seizure means that the signaling converter supplies a voltage of -60 volts to the C contact of the assigned output of the group selector GW. This is the case if the two transistors T1 and T2 of figure 2 are in the activated state. These two transistor stages form the switch designated by S1 in figure 1. The group selector GW carries out high-resistance testing, i.e. it connects the high-resistance winding P1 of relay P between said C

contact and ground. The relay P thereupon pulls-in and short-circuits the high-resistance winding P1 with its own contact p1. The resultant change in the relay current  $i$  effects a change in the logic level at the output of the transistor T7. This transistor T7, in conjunction with the transistor T5, forms the threshold value switch SW illustrated in figure 1. As a result of the change in the logic level at the output of the transistor T7, with the aid of the logic device LE, the two transistors T1 and T2 are switched into the off state and the two transistors T3 and T4 are switched into the on state. This measure effects a changeover from the first current source with the voltage source U1 and the series resistor R1 to the second current source with the voltage source U2 and the series resistor R2 and thus from the pull-in circuit to the holding circuit. The voltage source U2 has a terminal voltage  $u_2$  whose magnitude is significantly less than that of the terminal voltage  $u_1$  of the voltage source U1 ( $u_1 = -60$  volts,  $u_2 = -17$  volts). Consequently, a significantly smaller power loss results upon the application of the holding current through the use of the voltage source U2 instead of the voltage source U1.

The exemplary embodiment of the circuit arrangement according to the invention is discussed below, in which exemplary embodiment, even in the case of such a small power loss, the relay P does not drop out if an interference voltage is superposed on the holding current. For this purpose, firstly the construction and method of operation of the regulator Rg are described. In an advantageous embodiment, the transistor stage T5 is part of both the threshold value switch Sw and the regulator Rg. The two resistors R3 and R5 are connected to the junction point of the series resistors R1 and R2. The resistor R3 leads via the forward-biased diode D, via the resistor R8 and via the contacts of the group selector GW to the winding of the relay P. The

resistor R5 is connected to the emitter of the transmitter T5, whose base is connected to the junction point between the resistor R8 and the anode of the diode D.

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The series circuit formed by the resistor R3 with the diode D and the emitter circuit of the transistor T5 connected in parallel therewith form the input of the threshold value switch Sw and of the regulator Rg. The collector of the transistor T5 is connected to the base of the transistor T6 and is grounded via the series circuit formed by the resistors R6 and R7. The junction point of these two resistors is connected to the emitter of the transistor T6 and the base of the transistor T7, whose emitter is connected to ground. Said transistor T7 forms a switching stage with its resistor R13, the collector forming the output of the threshold value switch Sw. As mentioned above, said output indicates to the logic device LE, by means of a state change, if the relay P has pulled-in and thus initiates the changeover from the pull-in circuit to the holding circuit.

The current  $i$  amounts to about 50 times the collector current  $i_5$  of the transistor T5 ( $i \approx 50 \times i_5$ ). Accordingly, the relationship:  $R5 \approx 50 \times R3$  also results for the ratio of the resistors R3 and R5. The U/J characteristic curve of the base-emitter junction of the transistor T5 is simulated by means of the diode D. As a result of this measure, the abovementioned value of about 50 for the ratio  $i/i_5$  is maintained in a wide modulation range of the transistor T5. The bases of the two pnp transistors T1 and T3, whose emitters are grounded, are driven via the resistors R9 and R10, respectively, from the outputs LE2 and LE3, respectively, of the logic device LE. The collector of the transistor T1 is connected to the base of the transistor T2 via the resistor R11 and the collector of

the transistor T3 is connected to the base of the transistor T4 via the resistor R12. The emitter of the transistor T2 is connected to the negative pole of the voltage source U1 and the emitter of the transistor T4 is connected to the negative pole of the voltage source U2. The resistors R14 ... R17 serve for better blocking of the relevant transistor T1 ... T4. The collector of the transistor T6 is connected to the resistor R10 or output LE3 of the logic device LE via the resistor R4.

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The capacitor C1 is connected between the collector of the transistor T6 and the junction point between the base of the transistor T1 and the resistors R9 and R14. Said junction point forms the input and the collector-emitter path of the transistor T2 forms the output of the controllable resistor Rs. Thus, in this advantageous embodiment described, the transistor stages T1 and T2 form both the switch S1 and the resistor Rs, which is controllable in an analogous mode of operation. The capacitor C2 is connected between the collector of the transistor T1 and ground. Said capacitor serves for suppressing possible instabilities.

25 The case taken as a basis is the one in which the holding circuit is switched on, that is to say the relay P draws its holding current  $i=i_h$  from the voltage source U2 via the activated transistor T4. In this case, the transistor T6 is also activated, this transistor receiving its collector current from the negative control voltage - occurring at the output LE3 of the logic device LE - via the resistor R4. It is now assumed that an interference voltage is superposed on the holding circuit. Such an interference voltage may be, for example, a voltage having a frequency of 16 2/3 Hz or 50Hz that is coupled in from a power network via the C core. This superposed interference voltage causes the relay current i to be increased

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during the negative half-cycle of the interference voltage and decreased during the positive half-cycle. If the relay current  $i$  falls below a specific value during the occurrence of said positive half-cycle, then  
5 the voltage drop across the resistor R6 falls below the value of the base-emitter voltage required for activating the transistor T6, and the transistor T6 undergoes transition to its linear region. As a consequence thereof, the collector of the transistor T6  
10 assumes negative values, a charging current  $i_L$  flowing via the resistor R4 and the capacitor C1 to the junction point between the resistors R9 and R14 and the base of the transistor T1. This charging current causes the transistors T1 and T2 to be switched from the off  
15 state into the linear region and a current which counteracts the decrease in the relay current  $i$  to flow from the voltage source U1 into the relay circuit. The charging current  $i_L$  has a temporal profile which is proportional to the capacitance of the capacitor C1 and  
20 approximately the time derivative of the relay current  $i$ . The regulator Rg therefore has a D action. This action has the advantage that a particularly strong regulating operation commences in the event of pulsed dips in the current supplied by the current source J2.

25 If the voltage zero volts occurs at the output LE3 of the logic device LE, that is to say if the pull-in circuit is switched on, then the regulator Rg remains inactive.

30 The time constant formed from the resistor R4 and the capacitor C1 must be dimensioned such that a charging current  $i_1$  can flow for the longest expected duration of the current undershoot. In the exemplary embodiment, said time constant is designed for the duration  $t=30$  ms  
35 of a half-cycle of the lowest arising interference frequency of  $16 \frac{2}{3}$  Hz. For elucidation, these relationships are illustrated in a current/time diagram

in figure 3. In this case, an interference voltage of amplitude  $A$  is superposed on the holding current  $i = i_h$ . If the profile of the relay current  $i$  has reached the value  $i_r$ , then the regulating operation  
5 according to the invention commences and the current  $i$  remains constant until it assumes values greater than  $i_r$  again. For the case where use is not made of the arrangement for carrying out this regulating operation, the dashed profile is applicable instead of the  
10 constant section of the current profile  $i$ . In this case, the current  $i$  would fall below the value for the drop-out current  $i_f$  and the relay  $P$  would drop out.

A circuit arrangement designed for an interference  
15 frequency of  $16 \frac{2}{3}$  Hz, for example, can also process shorter interference pulses, for example positive half-cycles which originate from an interference frequency of 50 Hz. In this case, the transistor  $T6$  is activated again as early as at the end of the  
20 interference pulse and the regulating operation is ended correspondingly earlier owing to the absent charging current.

The invention also works with a relay which has only a  
25 single winding instead of the two windings  $P1$  and  $P2$ . In this case, it is necessary merely for the regulator  $Rg$  to be dimensioned accordingly. The invention can also be employed when corresponding electronic  
embodiments of a relay are used instead of an  
30 electromechanical relay.

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Accompanied by two sheets of drawings

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DRAWINGS SHEET 1

NUMBER :

28 09 905

Int.  $Cl^3$ :

H 01 H 47/04

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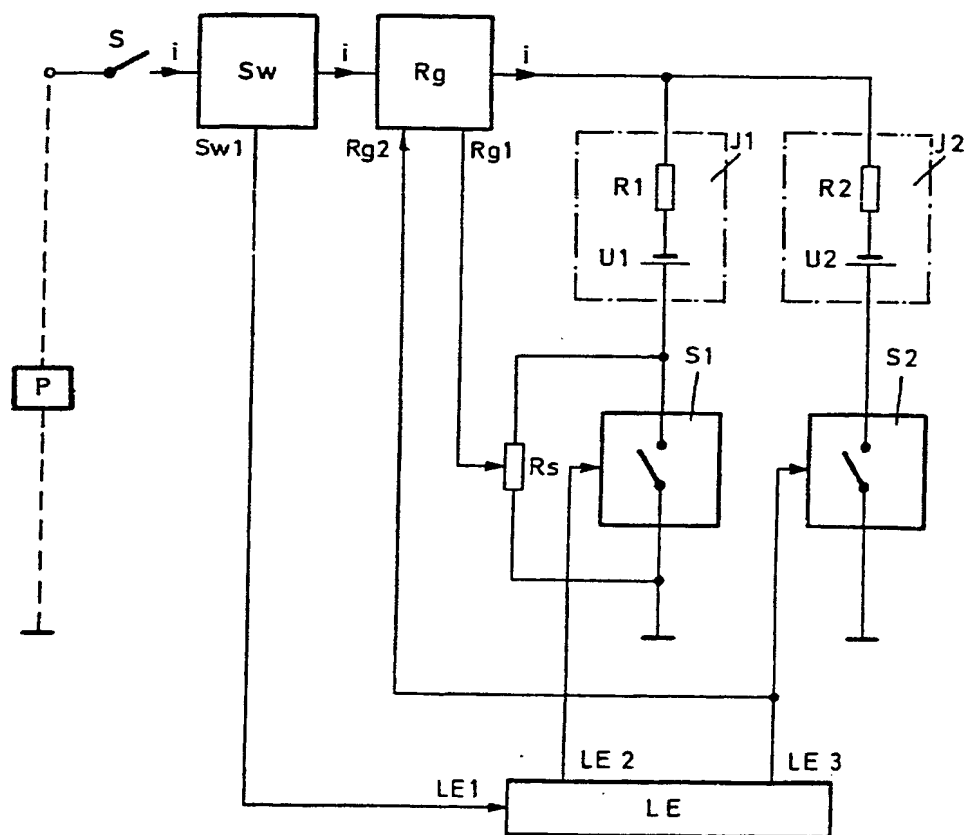


Fig. 1

DE 28 09 905

Circuit arrangement for the actuation of a switching magnet

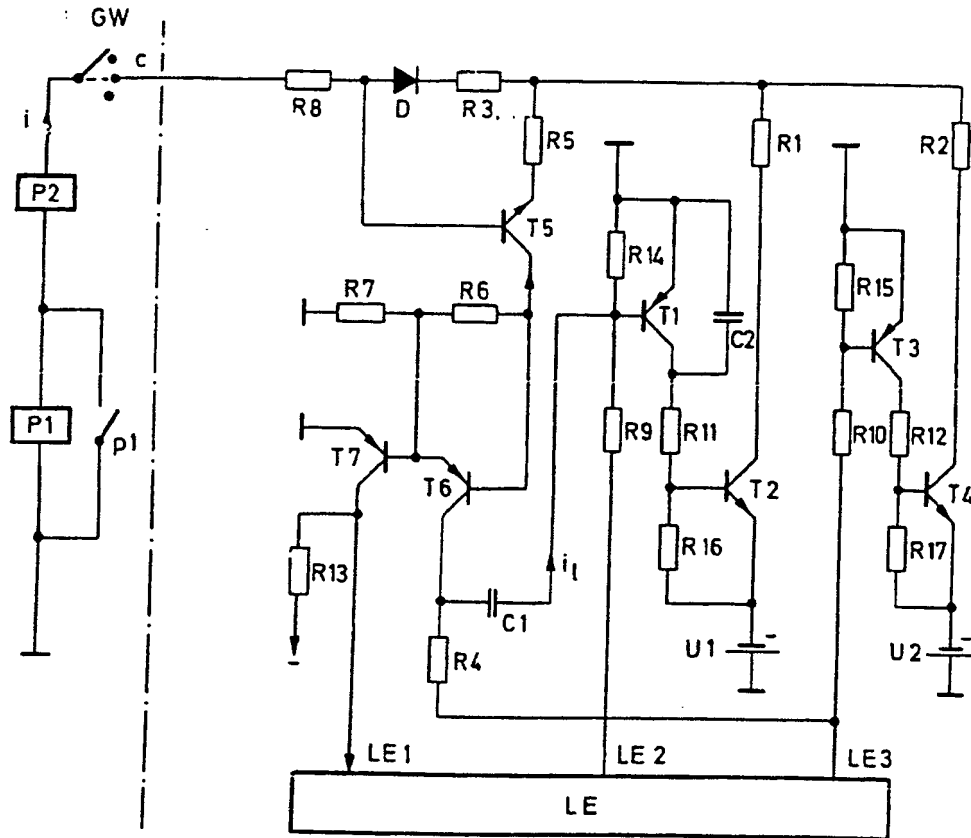


Fig. 2

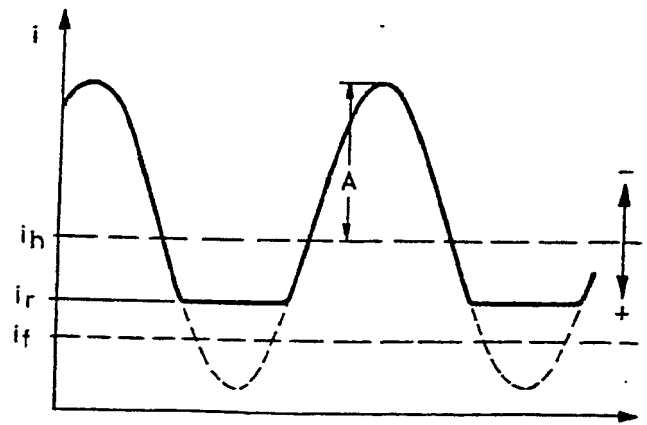


Fig. 3